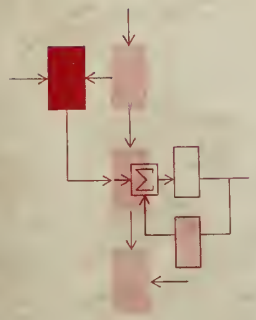

A HIGH-SPEED SAMPLE AND HOLD CIRCUIT

by

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BS Thesis May 18, 1962

(NESEP Program Thesis)

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Department of Electrical Engineering

A HIGH-SPEED SAMPLE AND HOLD CIRCUIT

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Craig Alan Bergman

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REQUIREMENTS FOR THE DEGREE OF
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Chairman, Departmental Senior Thesis Committee

A HIGH-SPEED SAMPLE AND HOLD CIRCUIT

by

Craig Alan Bergman

Submitted to the Department of Electrical Engineering on May 18, 1962 in partial fulfillment of the requirements for the degree of Bachelor of Science in Electrical Engineering.

ABSTRACT

A sample and hold circuit has been developed which is capable of sampling for periods as short as 10 usec over a ± 20v range. Proportional linearity is 0.1% and zero accuracy, noise, and drift are all less than ± 20 mv. The circuit will hold the sampled voltage for as long as 32 msec with a decay of less than 0.1% of the sampled voltage.

Thesis Supervisor..... Paul E. Gray .....

Title.....Assistant.Professor.of.Electrical.Engineering.....

ACKNOWLEDGEMENT

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Credit is due to Mr. Andrew Platais who drafted the figures, and to Miss Therese Bergeron who cheerfully assumed the burden of typing this thesis.

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CHAPTER I

INTRODUCTION

1.1 The PADIC

The PADIC, or Pulsed Analog and Digital Computer, is representative of a new class of computer employing features of both analog and digital machines.

In conventional analog machines, complex computations are performed continuously on continuous variables. This requires that an integrator be used for each integral appearing in the problem statement. The same is true for all operational functions.

In the PADIC system, however, by allowing the digital computer to control the routing and temporary storage of analog information, the computing elements are used on a time-shared basis. Routing and temporary storage of analog information are performed by sample gates and storage gates, respectively.

Control, bookkeeping, and some computations are performed by the digital machine. The program for the problem is entered and stored in the digital machine. Information is exchanged between the two machines by D-A and A-D converters.

1.2 The Storage Gate

This thesis is concerned with the design and construction of the storage gate for the PADIC system. An ideal storage gate is defined as having an output voltage which is equal to the input voltage during the enabled (or sampling) period, and which remains at that same value until the next enable period. The output voltage must be independent of what appears at the input between enable periods. Essentially, this is a zero-order hold, or sample and hold circuit.

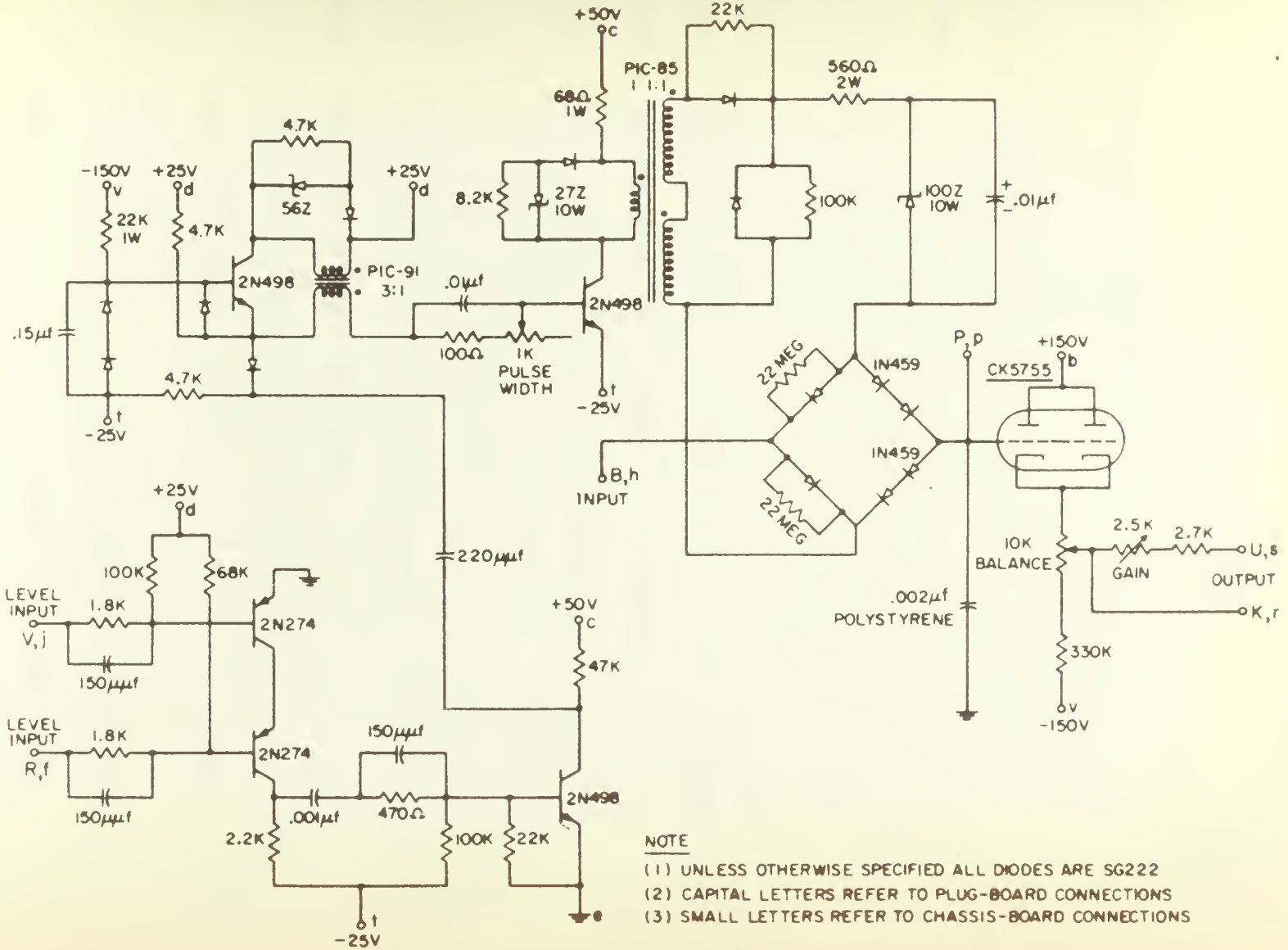
1.3 Storage Gate Specifications

The system requirements are that resolution and accuracy be one part in one thousand over a range of $\pm$ 20 volts, that computations be performed as fast as is compatible with the TX-0 or PDP-1 digital computer, and that the total problem be repeated at least 32 times per second.

This means that the storage gate must sample for no more than 10 usec, the cycle time of the PDP-1 computer, and hold for 32 msec with a zero accuracy of $\pm$ 20 mv and a proportional linearity of 0.1% over a range of $\pm$ 20v. Noise and drift must be less than $\pm$ 20 mv.

1.4 First Generation PADIC

The first generation of the PADIC system was demonstrated in August of 1960. The TX-0 digital computer was used with the pulsed-analog computer developed in this Laboratory. With this system, function generation was performed with accuracies approaching 1%. Fig. 1 shows the storage gate used in this system. This circuit required a driver capable of supplying $\pm$ 40 ma of current at its input. It would hold the desired output voltage within $\pm$ 20 mv for 20 msec, and had a linearity of 0.25% over a dynamic range of $\pm$ 20v.



NOTE

(1) UNLESS OTHERWISE SPECIFIED ALL DIODES ARE SG222
(2) CAPITAL LETTERS REFER TO PLUG-BOARD CONNECTIONS
(3) SMALL LETTERS REFER TO CHASSIS-BOARD CONNECTIONS

Fig. 1 The PADIC Storage Gate

CHAPTER II

CONFIGURATIONS AND ANALYSIS

2.1 Storage Gate Configuration

As may be seen from Fig. 1, the storage gate in the First Generation PADIC is open loop, and is therefore necessarily a linear device. Figure 2 shows this in block-diagram form. Here, during the enable period (sampler closed by decoder) the input voltage is placed on the capacitor. During the hold period, the impedance of the open sampler in parallel with the input impedance of the buffer is enough to maintain the voltage on the capacitor within $\pm$ 20mv for 20 msec. The buffer output is low impedance in order to provide a usable output during the hold period. The linearity of this device is 0.25%, limited by the non-linearity of the buffer at the negative end of the operating range. The two control signals going to this device are a select level, selecting one of many storage gates, and the enable pulse which fires a blocking oscillator that determines the duration of the enable period.

The new storage gate, shown in block diagram form in Fig. 3, grew out of a suggestion that the Miller integrator idea might be used in this application. Due to the closed

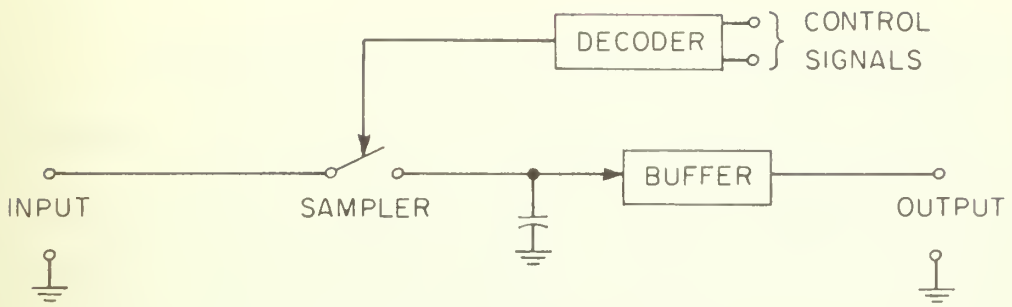


Fig. 2 PADIC Storage Gate

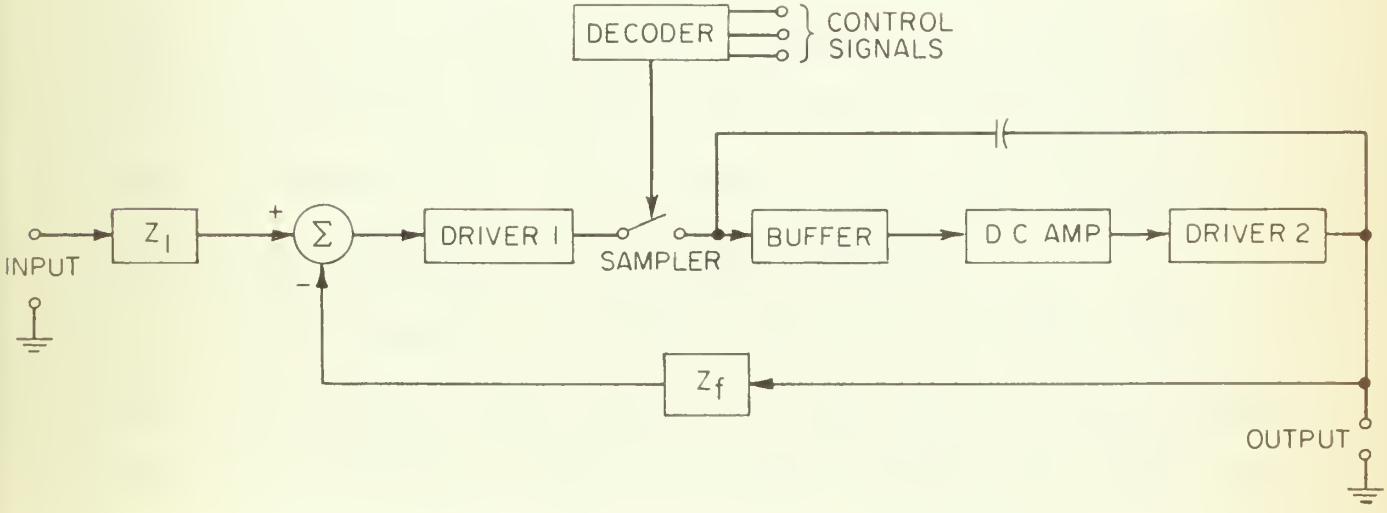


Fig. 3 New Storage Gate

loop configuration, the elements within the loop need no longer be linear, and drift may be tolerated in the output stages.

It was decided to use three control signals for this system. One is a select level, another an enable pulse, and the third a reset pulse. The two pulses go to all storage gates in the system, whereas the select level goes only to the selected storage gate. The time interval between the two pulses determines the duration of the enable period.

The input and feedback impedances, Z_1 and Z_f are equal so the overall gain is (negative) unity. Driver 1 is necessary to provide a low impedance charging path for that side of the capacitor. The buffer provides the required high input impedance, the d-c amplifier provides the loop gain, and driver 2 provides a low output impedance.

When the sampler is closed, the circuit looks like a unity gain operational amplifier. The output voltage appears across the capacitor since it is tied between the output and, essentially, the summing point.

When the sampler is open, the circuit looks like a Miller integrator, the output voltage equal to the capacitor voltage, independent of what appears at the input.

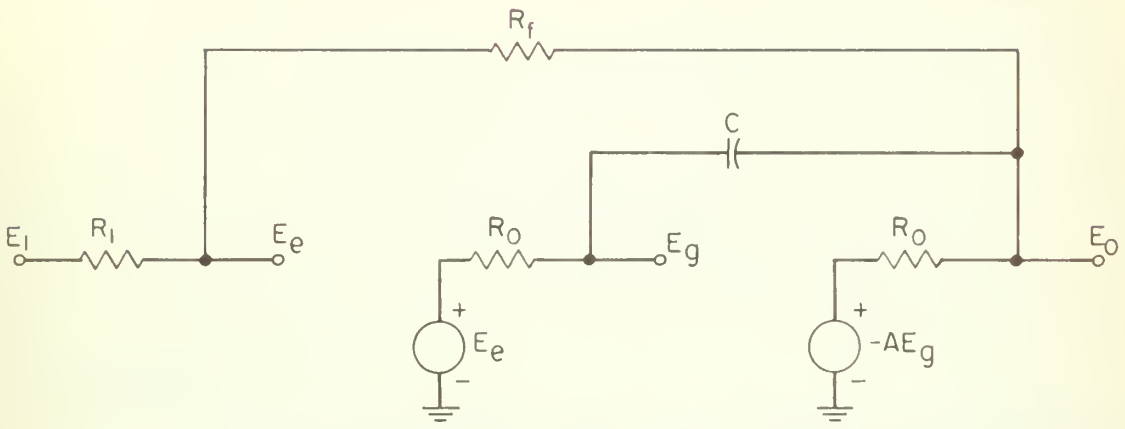


Fig. 4 Model for Enable State

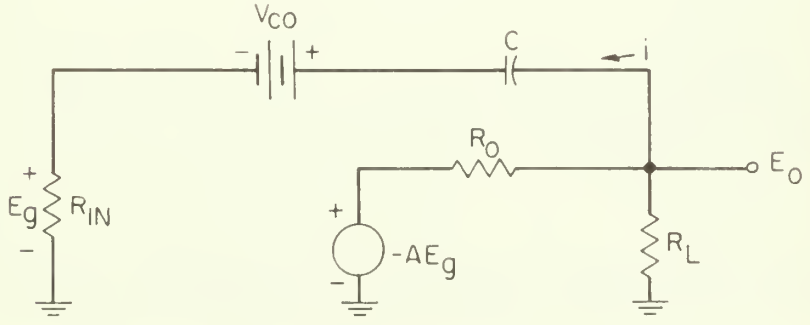


Fig. 5 Model for Hold State

An elementary analysis would indicate that during the enable period the charging time constant is 2 Ro C, where R_o is the output impedance of either driver, and that the hold time constant is $AR_{in}C$ where A is the gain of the d-c amplifier and R_{in} is the input impedance of the buffer. These two assertions will be proven in the next section.

2.2 Analysis

For purposes of analysis, the enable and the hold states will be treated separately.

For the enable state, the model shown in Fig. 4 will be used. R_1 and R_f are the input and feedback impedances, respectively, E_e is the error voltage at the summing point, the source E_e and R_o represent driver 1 (positive, unity gain), E_g is the input to the d-c amplifier, -A is the gain of the amplifier, and R_o represents the output impedance of drive 2.

By summing currents at the E_g node:

$$\frac{E_g - E_e}{Ro} = C \frac{d}{dt} (E_o - E_g) \tag{2.1}$$

where

$$E_o = - AE_g - \frac{R_o(E_g - E_e)}{R_o} \tag{2.2}$$

$$= - E_g(A + 1) + E_e \tag{2.3}$$

$$E_g = \frac{E_e - E_o}{A + 1} \tag{2.4}$$

Substituting into (2.1) and changing to Laplace transform notation gives:

$$\frac{\frac{E_e - E_o}{A + 1} - E_e}{R_o} = CS \left(E_o - \frac{E_e - E_o}{A + 1} \right) \tag{2.5}$$

$$E_e - E_o - E_e (A + 1) = R_o CS \left[E_o(A + 1) - E_e - E_o \right] \tag{2.6}$$

$$- AE_e - E_o = R_o CS(AE_o - E_e) \tag{2.7}$$

$$E_o(AR_o CS + 1) = E_e (R_o CS - A) \tag{2.8}$$

$$\frac{E_o}{E_e} = \frac{R_o CS - A}{AR_o CS + 1} \tag{2.9}$$

$$\frac{E_o}{E_e} = \frac{1}{A} \cdot \frac{S - \frac{A}{R_o C}}{S + \frac{1}{AR_o C}} \tag{2.10}$$

By summing currents at the E_e node:

$$\frac{E_e - E_1}{R_1} = \frac{E_o - E_e}{R_f} \tag{2.11}$$

$$(E_e - E_1)R_f = (E_o - E_e)R_1 \tag{2.12}$$

$$E_e(R_f + R_1) = E_oR_1 + E_1R_f \tag{2.13}$$

$$E_e = \frac{E_oR_1 + E_1R_f}{R_f + R_1} \tag{2.14}$$

Substituting (2.10) to eliminate E_e gives:

$$E_oA \frac{S + \frac{1}{AR_oC}}{S - \frac{A}{R_oC}} = \frac{E_oR_1 + E_1R_f}{R_f + R_1} \tag{2.15}$$

$$E_o \left(A \frac{S + \frac{1}{AR_oC}}{S - \frac{A}{R_oC}} - \frac{R_1}{R_f + R_1} \right) = E_1 \frac{R_f}{R_f + R_1} \tag{2.16}$$

$$\frac{E_o}{E_1} \frac{R_f}{\left[A \frac{S + \frac{1}{AR_oC}}{S - \frac{A}{R_oC}} (R_f + R_1) \right] - R_1} \tag{2.17}$$

This becomes:

$$\frac{E_o}{E_1} = R_f \frac{S - \frac{A}{R_oC}}{A(R_f + R_1)\left(S + \frac{1}{AR_oC}\right) - R_1\left(S - \frac{A}{R_oC}\right)} \tag{2.18}$$

$$= \frac{R_f\left(S - \frac{A}{R_oC}\right)}{\left(AR_f + (A-1)R_1\right)\left[S + \frac{1}{R_oC}\left[R_f + R_1(A+1)\right]\right]} \qquad (2.19)$$

which gives

$$\frac{E_o}{E_1} = \frac{R_f}{AR_f + (A-1)R_1} \cdot \frac{S - \frac{A}{R_oC}}{S + \frac{1}{R_oC}\left[\frac{R_f + (A+1)R_1}{AR_f + (A-1)R_1}\right]} \qquad (2.20)$$

as the impulse response of the system. For the step response this gives:

$$\frac{E_o}{E_1} = \frac{R_f}{AR_f + (A-1)R_1} \cdot \frac{1}{S} \cdot \frac{S - \frac{A}{R_oC}}{S + \frac{1}{R_oC}\left[\frac{R_f + (A+1)R_1}{AR_f + (A-1)R_1}\right]} \qquad (2.21)$$

In the time domain this becomes:

$$E_o(t) = \frac{-AR_fE_1\ u_{-1}(t)}{(A+1)R_1 + R_f}\left(1 - e^{-t/\tau}\right) + \frac{R_fE_1\ u_{-1}(t)}{AR_f + (A-1)R_1}\, e^{-t/\tau} \qquad (2.22)$$

where $\tau = \frac{AR_f + (A-1)R_1}{R_f + (A+1)R_1} R_oC$ (2.22a)

If $A \gg 1$ and $R_1 = R_f$

$$E_o(t) = -E_1\ u_{-1}(t)\left(1 - e^{-\frac{t}{2R_oC}}\right) \qquad (2.23)$$

which is the expected result.

For the hold state the model shown in Fig. 5 will be used. Here Vco is the voltage across the capacitor at the beginning of hold time and R_{in} is the input impedance of the buffer. Also, the effects of loading the output (R_1) will be considered.

$$i = \frac{d}{dt} (E_o - Vco - E_g) C \tag{2.24}$$

where

$$E_g = iR_{in} \tag{2.25}$$

and

$$E_o = - AE_g - R_o \left(i + \frac{E_o}{R_\ell} \right) \tag{2.26}$$

combining gives:

$$E_o = AiR_{in} - R_o \left(i + \frac{E_o}{R_\ell} \right) \tag{2.27}$$

and

$$i = \frac{d}{dt} \left(E_o - Vco - iR_{in} \right) C \tag{2.28}$$

In Laplace transform notation this becomes:

$$i = CS \left(E_o - Vco - iR_{in} \right) \tag{2.29}$$

Expanding and substituting from (2.25) and (2.26) gives:

$$i (1 + R_{in} CS) = CS E_o - CS Vco \tag{2.30}$$

$$E_o = i (- AR_{in} - R_o) - E_o \frac{R_o}{R_\ell} \tag{2.31}$$

$$E_o = \frac{CS\ E_o - CS\ Vco}{1 + R_{in}\ CS}\left(- AR_{in} - R_o\right) - E_o \frac{R_o}{R_\ell} \qquad (2.32)$$

$$E_o \left(1 + \frac{(AR_{in} + R_o)CS}{1 + R_{in}CS} + \frac{R_o}{R_\ell}\right) = \frac{AR_{in} + R_o}{1 + R_{in}CS}\ CS\ Vco \qquad (2.33)$$

which gives:

$$\frac{E_o}{Vco} = \frac{\dfrac{(AR_{in} + R_o)}{1 + R_{in}\ CS}\ CS}{1 + \dfrac{R_o}{R_\ell} + \dfrac{(AR_{in} + R_o)}{1 + R_{in}\ CS}\ CS} \qquad (2.34)$$

as the impulse response. The step response becomes:

$$\frac{E_o}{Vco} = \frac{\dfrac{AR_{in} + R_o}{1 + R_{in}CS}\ C}{1 + \dfrac{R_o}{R_\ell} + \dfrac{(AR_{in} + R_o)}{1 + R_{in}CS}\ CS} \qquad (2.35)$$

$$= \frac{(AR_{in} + R_o)\ C}{\left(1 + \dfrac{R_o}{R_\ell}\right)(1 + R_{in}CS) + (AR_{in} + R_o)CS} \qquad (2.36)$$

$$= \frac{(AR_{in} + R_o)C}{\left(R_{in} + \frac{R_{in}R_o}{R_\ell} + AR_{in} + R_o\right)CS + \frac{R_o}{R_\ell} + 1} \qquad (2.37)$$

$$\frac{E_o}{Vco} \quad \frac{AR_{in} + R_o}{(A + 1)R_{in} + R_o\left(1 + \frac{R_{in}}{R_\ell}\right)} \cdot \frac{1}{S + \frac{(R_o + R_\ell)\,C}{(A+1)R_{in}R_\ell + R_o(R_\ell + R_{in})}} \qquad (2.38)$$

In the time domain this becomes:

$$E_o(t) = Vco \quad u_{-1}(t) \quad \frac{AR_{in} + R_o}{(A + 1)R_{in} + R_o\left(1 + \frac{R_{in}}{R_\ell}\right)} e^{-t/\tau} \qquad (2.39)$$

where

$$\tau = \frac{(A + 1)R_{in}R_\ell + R_o\,(R_\ell + R_{in})}{R_o + R_\ell} C \qquad (2.39a)$$

If $A \gg 1$ and $R_\ell \gg R_o$

$$E_o(t) = Vco \quad u_{-1}(t)e^{-\frac{t}{AR_{in}C}} \qquad (2.40)$$

which is, again, the expected result.

CHAPTER III

SEMICONDUCTOR DEVICES

3.1 The Field-Effect Transistor

Before the closed loop configuration was suggested, some time was spent looking for a way to improve upon the buffer in the open loop system of Fig. 2. It appeared that the field-effect transistor would be suitable for this application.

The field-effect transistor is a voltage operated device with an input impedance greater than 10 megohms at d-c for negative grid to cathode voltage. The device has characteristics which resemble those of a triode when the anode to cathode voltage is below a level called the pinch-off voltage, and which resemble those of a pentode at higher voltages. When cut off the device has an anode to cathode resistance of 100 megohms or more shunted by 5 pf of capacitance. When the grid to cathode voltage equals zero, the anode to cathode impedance is approximately 2K. The device is made of silicon and has the normal temperature effects associated with that material. Leakage currents are on the order of 1.0 na at room

temperature. Transconductances of 100 to 1200uA/v are available.

When the emphasis shifted to the closed loop configuration with its associated sub-miniature vacuum tube drivers, it was decided, due to the prohibitive cost of the field effect transistor, that another sub-miniature vacuum tube would be a suitable buffer. The possible future uses of this device will be mentioned in the section on recommendations.

3.2 The PNP Symmetrical Transistor

This device, sometimes called a bilateral transistor, was considered, and ultimately used, as a sampling device. It has an "on" resistance of 10 ohms, an offset voltage of 4-6 mv, an "off" resistance of 1 gigohm or more, and leakage currents of 1 na or less. The d-c current gain in either direction is about 6 for the device used in this circuit, the 2N1640. More will be said about this device in the section on the sampler.

CHAPTER IV

CONSTRUCTION OF THE STORAGE GATE

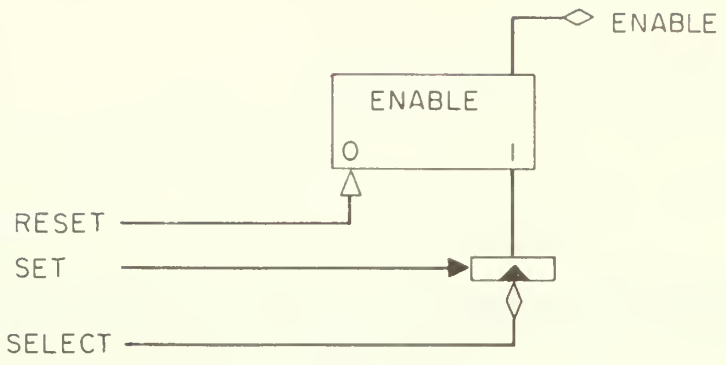
4.1 The Decoder*

Since the pulsed analog equipment is being designed to work under the control of either the TX-0 or PDP-1 digital computer (both of which use essentially the same circuitry), it is desirable to use the same logic circuitry for the decoder. This eliminates the need for any buffers between the digital computer and the pulsed analog decoders.

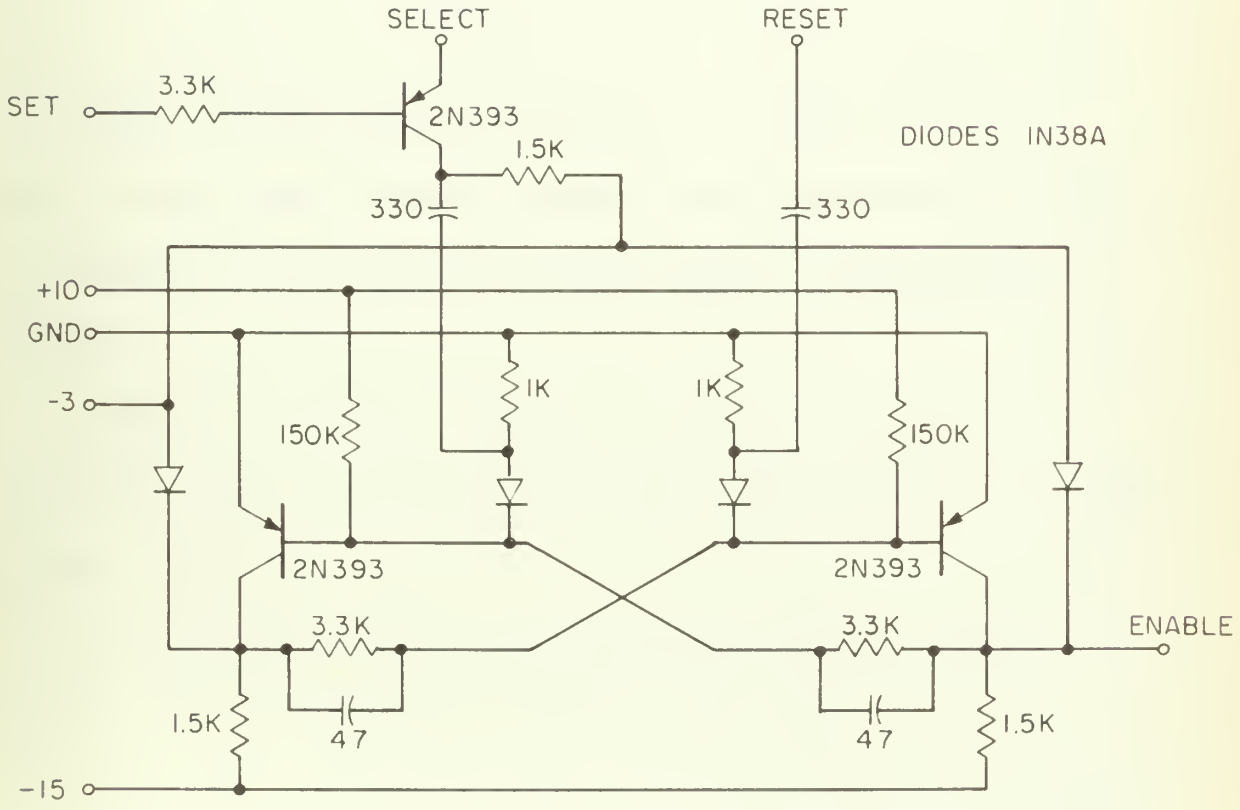
As was stated earlier, it was decided that this system would use a select level to designate the selected storage gate, and enable and reset pulses going to all storage gates. The logical product of the select level and the enable pulse sets the flip-flop controlling the selected gate. The reset pulse resets all flip-flops, the output of each flip-flop being used as the enable command to an individual sampler.

The decoder block diagram and circuit are shown in Fig. 6. The select level must be true at 0v and false

* This is not to be confused with the PADIC system decoder which is a d-a converter.



(a) Decoder Logic



(b) Decoder Circuit

Fig. 6

at -3v. The set pulse must be negative and the reset pulse, positive. The enable command from the decoder is true at 0v and false at -3v.

4.2 The Sampler

The PNP symmetrical transistor being used requires a negative voltage at the base for turn-on and a positive voltage for turn-off. These voltages must be greater in magnitude than the largest possible signal voltages appearing at the sampler. In addition, the turn-on signal must be capable of supplying a current of at least 1/B times the maximum signal current passing thru the sampling device, B being the bidirectional current gain of the sampling device.

Figure 7 shows the circuitry used for the sampler. The enable input is at ground in the enable state and at -3v in the hold state.

The Thevenin and Norton equivalents of the sampler are 20v and 9 kilohms for the hold state and 1.5 ma and 68 kilohms for the enable state. The analysis for the hold state is very straightforward since the 2N699 is cut off. In the enable state the voltage at the emitter-collector terminals of the 2N1640 is zero since these terminals are

essentially the same as the summing point of the closed loop. At the same time, the 2N699 is drawing collector current such that its collector-ground voltage is about + 10v. With only 10v across the 56v Zener diode, it appears as an open circuit. This explains the increased output impedance in the enable state.

When the symmetrical transistor is switched, there is some capacitive coupling between the base and the signal path. This is of no concern when switching into the enable state since the low impedance drivers charge the memory capacitor to the new desired voltage. But when switching into the hold state, some extra charge is dumped onto the memory capacitor creating an error voltage on the capacitor. This error voltage is very much dependent on the voltage at the collector-emitter terminals of the symmetrical transistor, so if this device were to be used in an open loop application the error voltage would give results which would be unsatisfactory.

Since the application in this circuit is at the summing point of a closed loop, the voltage here is always zero just prior to switching into the hold state. The error

voltage is therefore independent of the input voltage and can be compensated for by a change in the zero set equal to the error voltage.

4.3 The Buffer

The buffer input has a very high impedance to preserve the charge on the memory capacitor while in the hold state. This circuit is shown in Fig. 8.

Grid current curves for most vacuum tubes have a region near zero volts on the grid within which grid current can be made to flow in either direction. And the symmetrical transistor, while in the hold state, has a small but finite reverse bias current flowing from the base, through the device, and toward the buffer and memory capacitor. If these two currents can be made equal to each other, the result would be no current into or out of the memory capacitor, hence no voltage decay while in the hold state. These currents are made equal by varying the operating point, i.e., varying the grid voltage, of the buffer by means of adjusting its plate voltage. If temperature stability becomes a problem, a back-biased germanium diode tied from the buffer grid to a negative voltage should take care of it. A detailed explanation of this procedure is

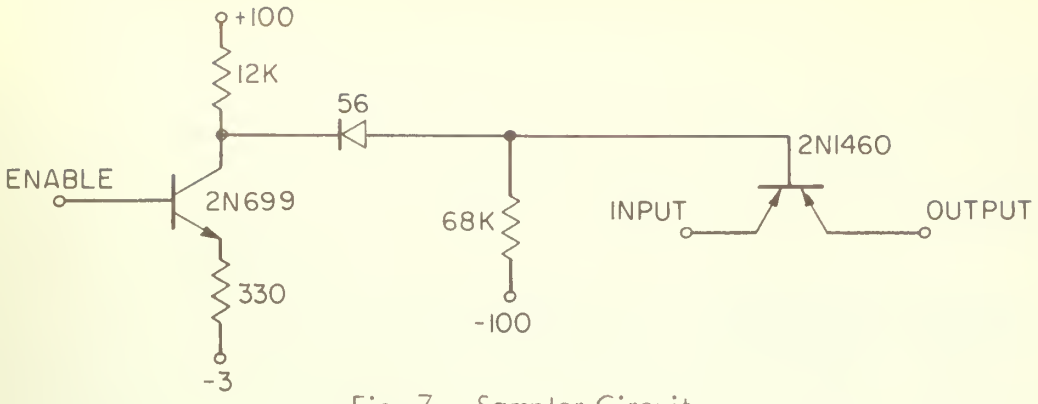


Fig. 7 Sampler Circuit

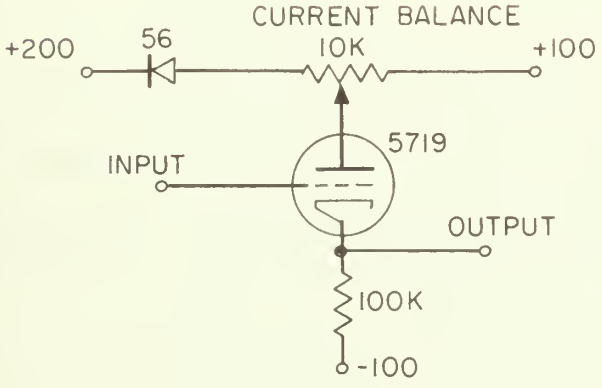


Fig. 8 Buffer Circuit

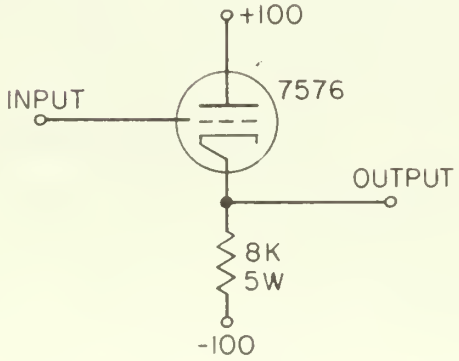


Fig. 9 Driver Circuit

given in Appendix A. With this method a large capacitor is not necessary to achieve a low rate of voltage decay.

4.4 The Drivers

The two drivers are simply low impedance cathode followers. Figure 9 shows the driver circuit. Here there was a trade-off between circuit complexity and a low quiescent current. If a quiescent current less than the maximum charging current was desired, Class B operation would have been necessary, requiring two tubes per driver. Since the buffer arrangement made possible the use of a small capacitor, allowing small charging currents, Class A operation was decided upon. The quiescent current is about 12.5 ma per driver.

4.5 The D-C Amplifier

A Philbrick K2-X was decided upon both for economy and ease of handling. This amplifier claims a d-c gain of 30,000 and a unity gain bandwidth of over 250 kc.

4.6 The Complete Storage Gate

Figure 10 shows the storage gate in its final form. The experimental results obtained with this circuit will be discussed in the next chapter.

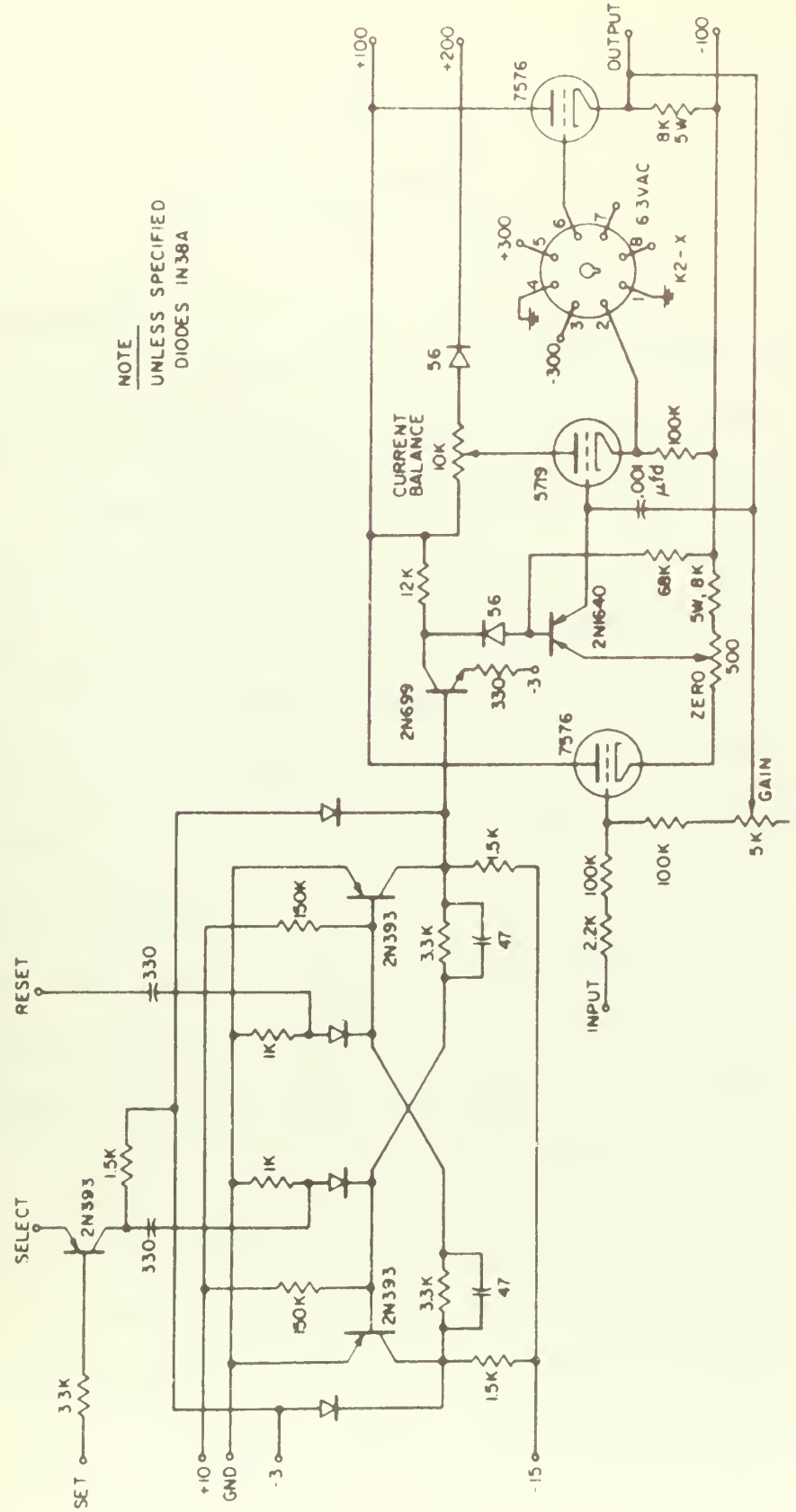


Fig. 10 The Complete Storage Gate

CHAPTER V

EXPERIMENTAL RESULTS

5.1 Measurements

The complete storage gate circuit, as shown in Fig. 10, is capable of a 40v change in output voltage, either positively or negatively, within the alloted 10 usec enable period. The limiting factor here is the rise time of the K2-X plus the settling time of the circuit. The output voltage is within 0.1% of the input voltage, except for a change of sign. Spot checks over an eight-hour period indicate that drift is less than $\pm$ 20 mv with the use of 0.002% power supplies at the $\pm$ 100v terminals. Noise is less than 10 mv rms. The current requirement is 30 ma at the $\pm$ 100v terminals. The sensitivity to power supply variations is -0.17* for both the +100v supply and the -100v supply. This means that with the input grounded, and with the 0.05% power supplies, the output voltage may vary as much as 17 mv due to external effects. Better regulation may be obtained at the expense of better supplies. There is some coupling between the input and output while the circuit is in the

* A +1v change in supply voltage will change the output by -0.17v.

hold state. This coupling causes a 10 mv change at the output for a 40v change at the input. This effect has been traced to the capacitance of the sampling device. It is, however, within tolerable limits.

It would appear that the drift problem might be reduced by utilizing chopper stabilization. This approach was investigated and the conclusion was that there is no voltage node in the circuit which gives a continuous representation of drift, eliminating the possibility of using chopper stabilization.

It should be noted that the entire circuit, including the control circuit, is d-c and may be operated at any speeds up to and including those specified.

5.2 Recommendations

If it becomes imperative for the circuit to be transistorized, the field-effect transistor, temperature compensated, could serve as the buffer.

This circuit could be made to operate faster by utilizing a faster d-c amplifier. The capacitor size is determined by the speed desired and the available charging current. There are two current limiting factors. One is the driver circuitry and the other is the sampler circuit.

By proper manipulation of all these factors, faster operation should be obtained.

5.3 Summary

A sample and hold circuit has been developed which is capable of sampling for periods as short as 10 usec over a ± 20v range. Proportional linearity is 0.1% and zero accuracy, noise, and drift are all less than ± 20 mv. The circuit will hold the sampled voltage for as long as 32 msec with a decay of less than 0.1% of the sampled voltage.

APPENDIX A

THE METHOD OF PARAMETRIC VARIATION OF THE OPERATING LOCUS

A new graphical analysis of the cathode follower has been developed and will be called the method of parametric variation of the operating locus. This method has the advantage of allowing the user to easily visualize the effect that a parameter change will have on the operating locus.

The circuit used is that of Fig. 9, and the three variable parameters are B^+, B^-, and the cathode resistor R_k. The method is illustrated in Figs. A-1, A-2, and A-3. All three figures have a common load line, operating point, and operating locus (unprimed labels). This common mode assumes a B^+ of 200v, a B^- of -100v, and an R_k of 8 kilohms. The tube curves are for the 7576 subminiature tube.

The bottom scale on all three drawings is the E_o-E_1 scale, where E_o is the output voltage and E_1 is the input voltage. The difference between E_o and E_1 is the grid voltage and on the E_o- E_1 scale this is negligible. A glance at Fig. 9 will show that E_o is always equal to B^+ minus the plate voltage. So if the E_o- E_1 scale is positioned

such that the voltage used for B^+ is placed under the corner where the plate voltage equals zero, the input and output voltages can be read from anywhere on the tube curves. The B^- voltage may be indicated on this same scale and the load line may then be drawn between B^- and B^+ as usual. The operating loci are for a capacitive load (to ground) and a square wave input between $\pm$ 20v.

Figure A-1 shows what happens to the operating locus when B^- is changed from -100v to -40v. The load line slides to the left and the operating locus slides down.

Figure A-2 shows what happens when R_k is changed from 8 kilohms to 4 kilohms. The slope of the load line becomes more steep and the operating locus moves up and expands in the vertical direction. For the new value of R_k the initial charging current is 18 ma (a' to b') for the negative step at the input, and 23 ma (c' to d') for the positive step.

Figure A-3 shows what happens when B^+ is changed from + 200v to + 100v. Here the entire $E_o = E_1$ scale is shifted to the left until the new value of B^+ comes under the lower left corner of the tube curve chart. This has the effect of shifting both the load line and the operating locus to the left.

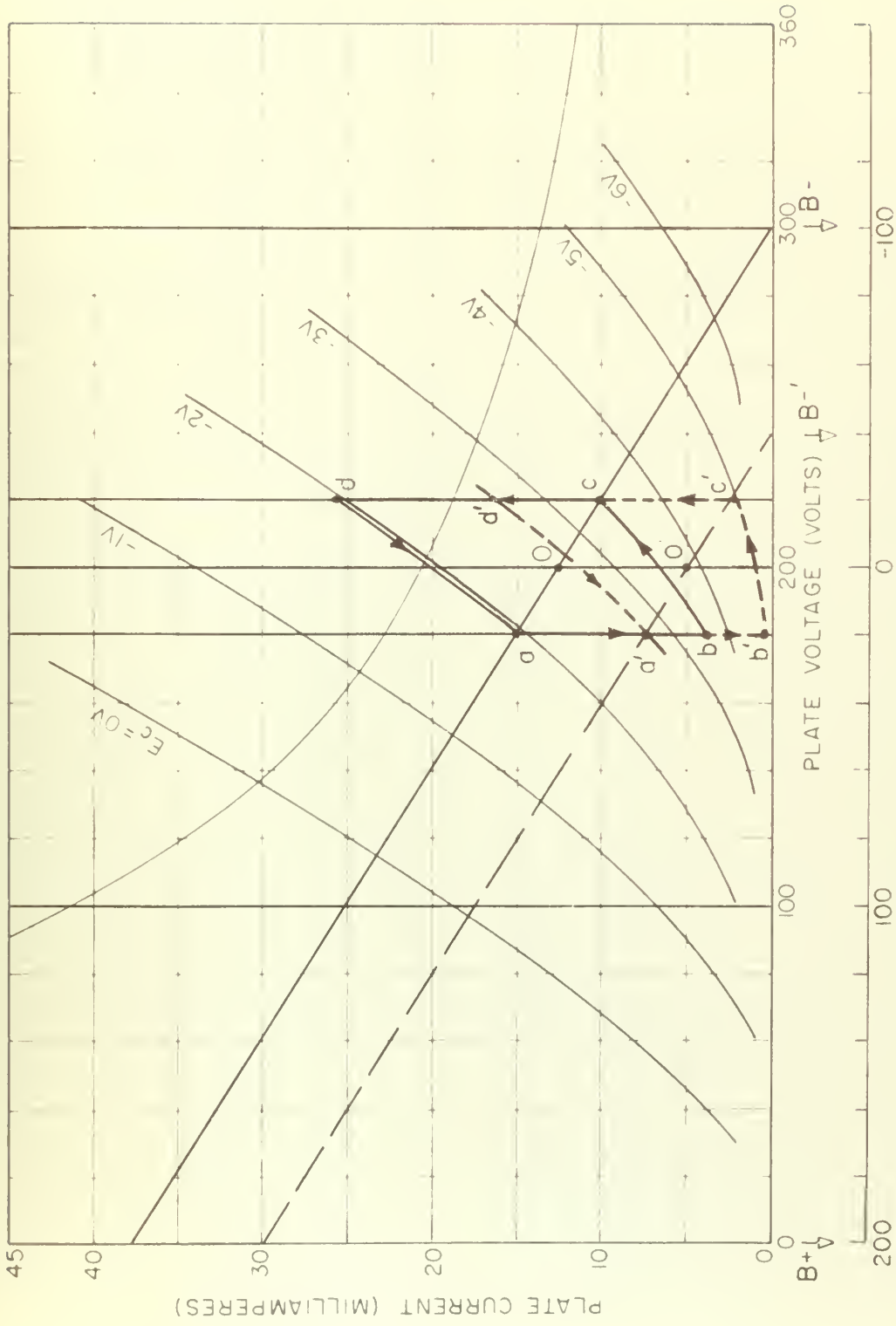


Fig. A-1 Change in B^-

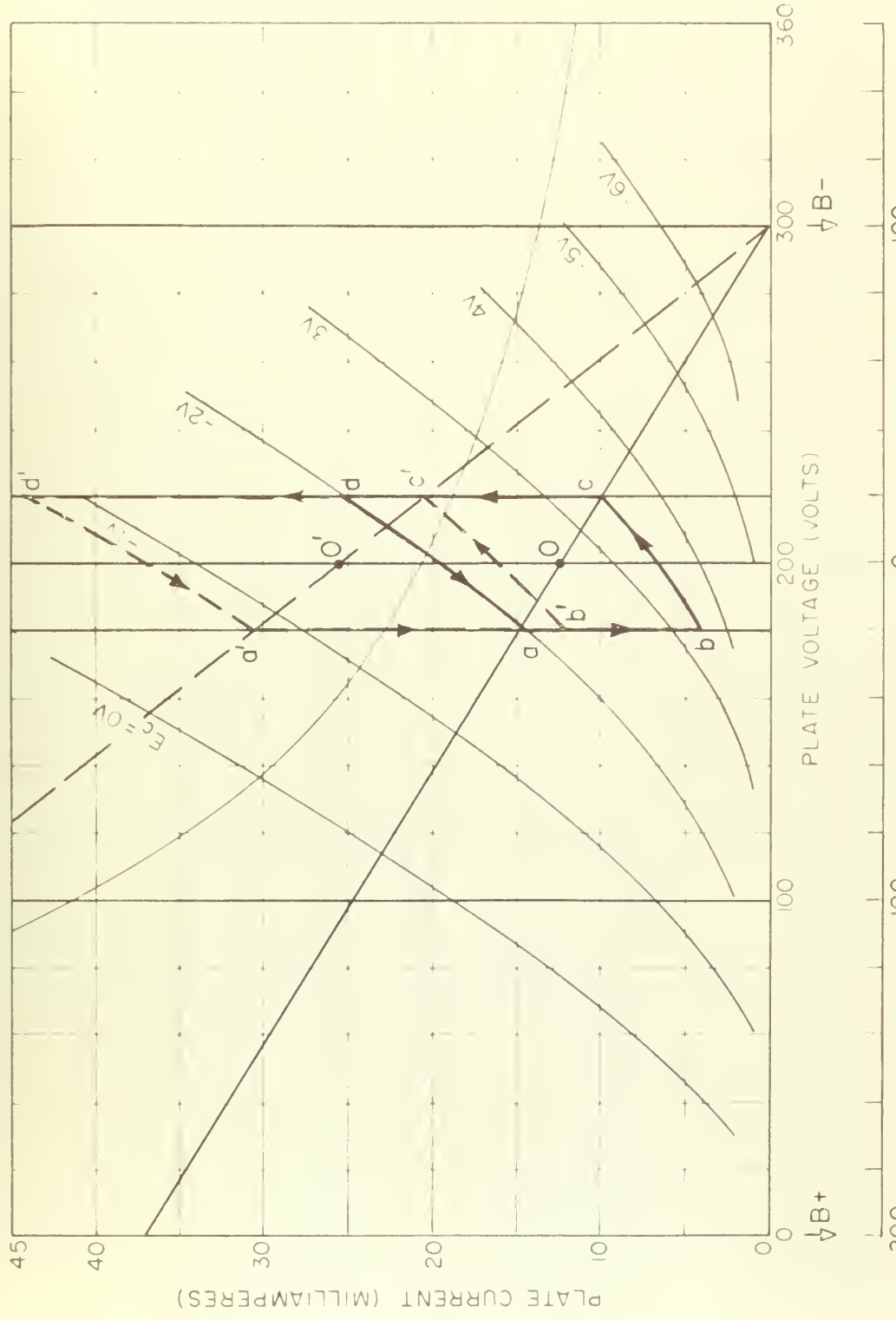


Fig A-2 Change in R_K

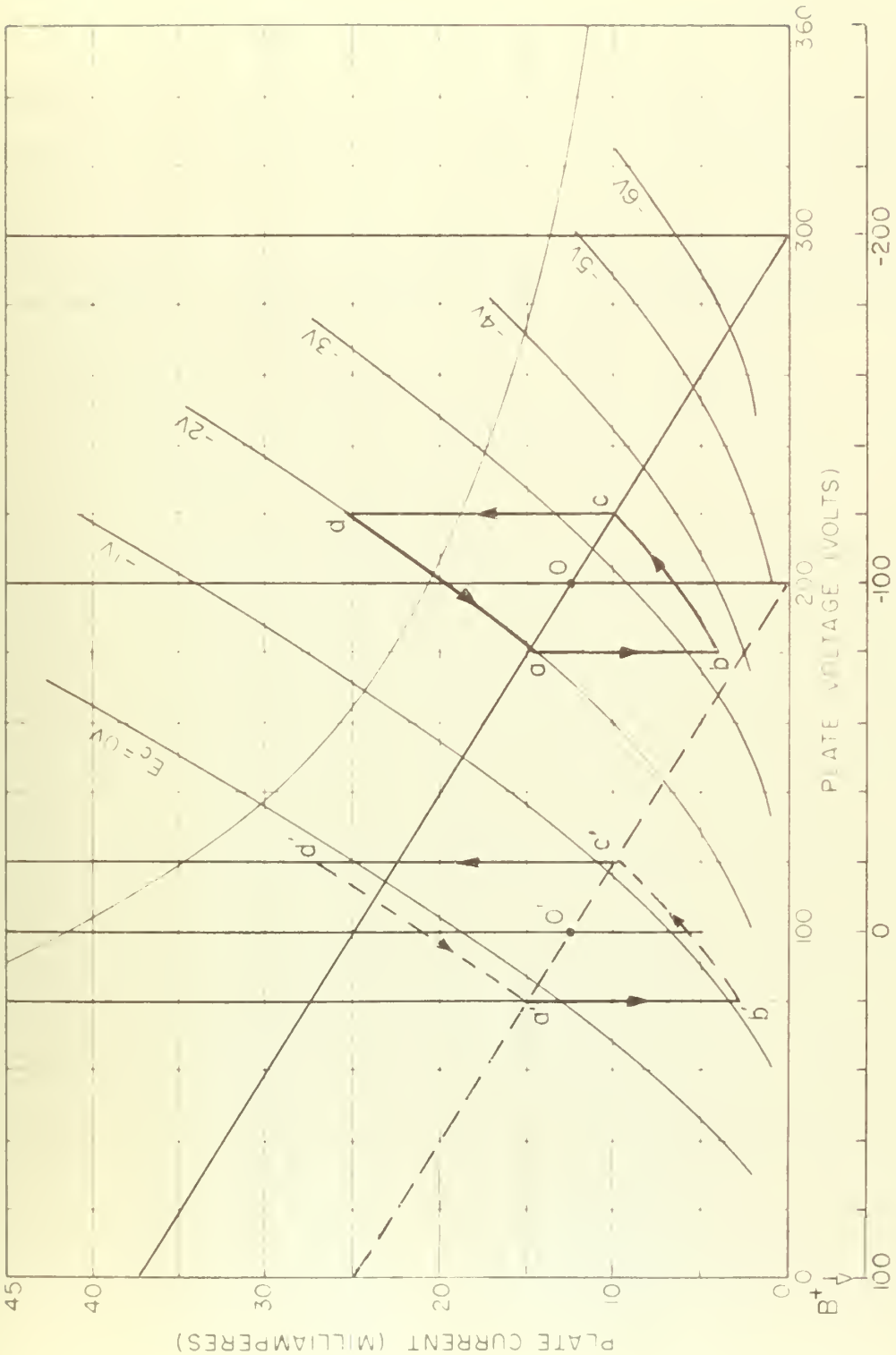


Fig. A-3 Change in B^+

As can be seen from the figures, this method of parametric variation of the operating locus has the distinct advantage of showing to the user, in a straightforward manner, what will be the effects of parameter changes. This method is particularly useful in determining how to get the most performance out of Class A drivers.

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